1.2MHz 1.5A Synchronous Step-Down Converter with Two LDOs

General Description

The RT8023 combines two low dropout (LDO) linear regulators and a step-down converter with an input voltage range of 2.6V to 5.5V. Each output voltage is adjustable from 0.8V to 5V. With independent Enable and Power-Good pins for each regulator, it is easy to control the power up sequence, which is important in some applications.

The LDO has an independent input and is capable of delivering up to 700mA(LDO1) and 350mA(LDO2) output currents with ultra-low dropout. The LDO has high PSRR and can work with low-ESR space saving ceramic capacitors. All these make it Ideal for portable RF and wireless applications with demanding performance and space requirements. Other features include high output accuracy, current limiting protection, and 40μs fast turn-on time.

The step-down converter is a 1.2MHz PWM, current mode converter. Its high switching frequency allows the use of tiny, low cost capacitors and inductors 2mm or less in height. Internal power switches with low on-resistance increase efficiency and eliminate the need for external Schottky diodes. The converter can run at 100% duty cycle for low dropout operation that extends battery life in portable systems.

Ordering Information

RT8023 □□

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Converter Input Voltage Range : 2.6V to 5.5V, LDO Input Voltage Range : 2.4V to 5.5V**
- **Low-Noise LDO for RF Application**
- **Ultra-Fast Response in Line/Load Transient**
- **LDO Turn-On Time Less Than 40us**
- **Only 1μF LDO Output Capacitor Required for Stability**
- **Current Limiting Protection**
- **1.5A, High Efficiency Step-Down Converter**
- **1.2MHZ Constant Switching Frequency**
- **Low $R_{DS(ON)}$ Internal Switches**
- **No Schottky Diode Required**
- **0.8V Reference Allows Low Output Voltage**
- **Low Dropout Operation : 100% Duty Cycle**
- **Internally Compensated**
- **< 2μA Shutdown Current**
- **Power Good Output Voltage Monitor**
- **Internal Soft-Start for PWM Converter**
- **Easy Power Sequence Control**
- **Over Temperature Protection**
- **Short Circuit Protection**
- **Thermally Enhanced 24-Lead WQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

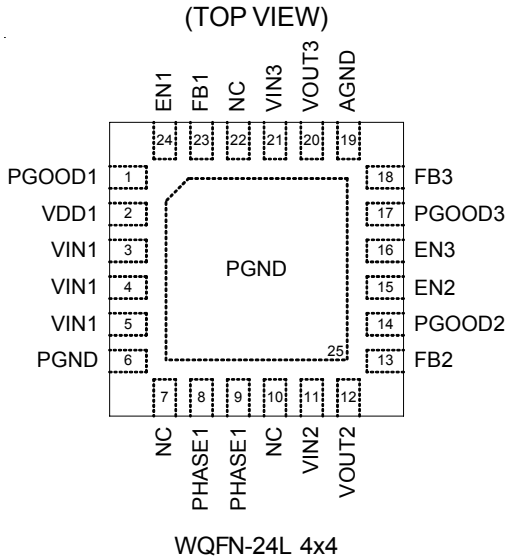
Applications

- Portable Instruments
- Microprocessors and DSP Core Supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards
- Digital Cameras

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configurations



WQFN-24L 4x4

Typical Application Circuit

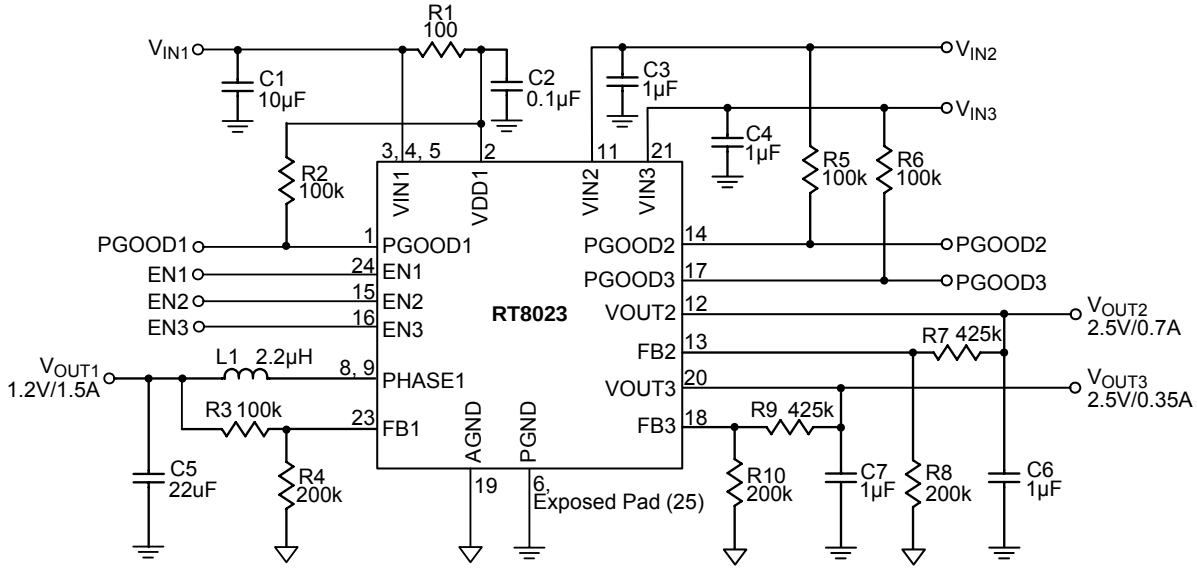


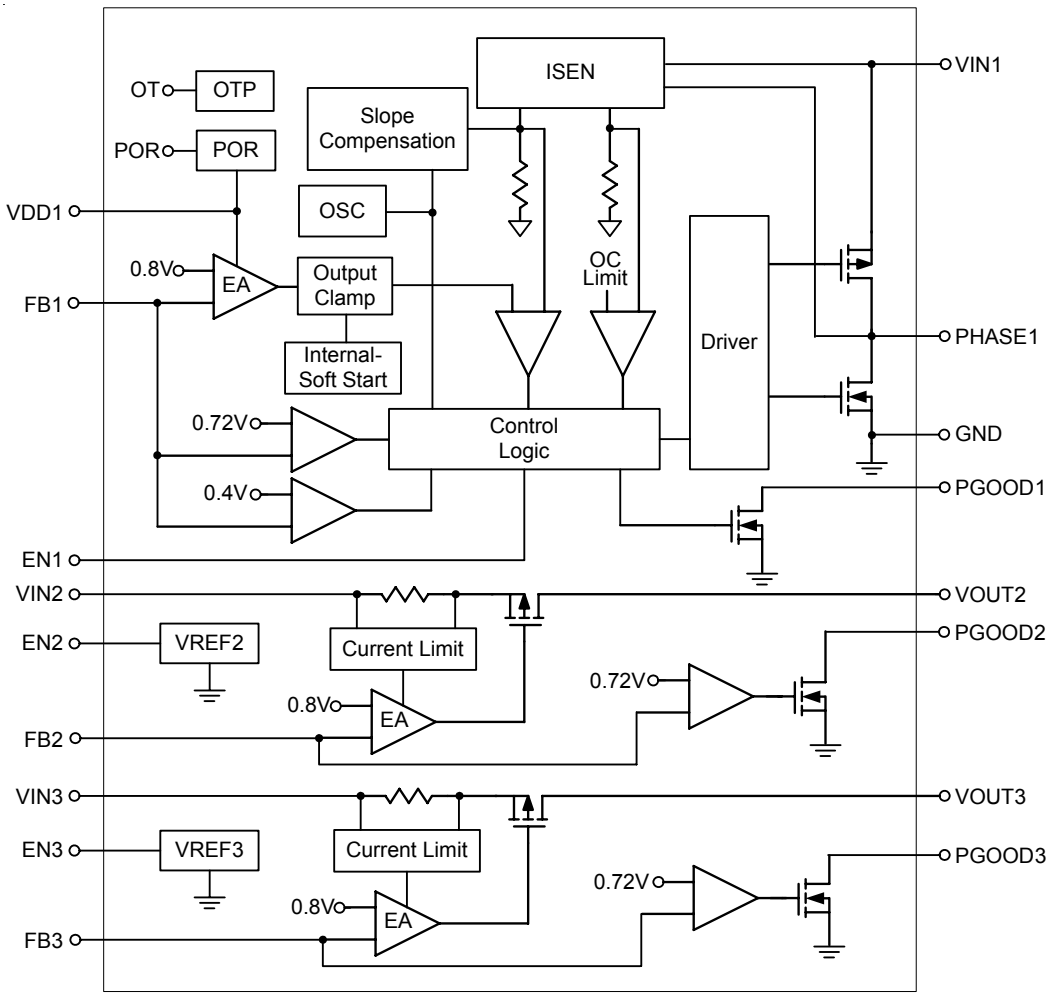
Figure 1. 1.2V Output Step-Down Converter and Dual 2.5V Output Regulators

Note : Must to use ceramic X5R/X7R capacitors.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGOOD1	Power Good Indicator of step-down converter. Open-drain logic output that is opened when the output voltage exceeds 90% of the regulation point.
2	VDD1	Signal Input Supply. Decouple this pin to GND with a capacitor. Normally VIN1 is equal to VDD1. Keep the voltage difference between VDD1 and VIN1 less than 0.5V.
3, 4, 5	VIN1	Power Input Supply of step-down converter. Decouple this pin to GND with a capacitor.
6, 25 (Exposed Pad)	PGND	Power Ground. Must be soldered to PCB ground for electrical contact and optimum thermal performance. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
8, 9	PHASE1	Internal Power MOSFET Switches Output of step-down converter. Connect this pin to the inductor.
11	VIN2	Power Input Supply of LDO1. Decouple this pin to GND with a 1Uf or greater capacitor.
12	VOUT2	Output of LDO1. A 1Uf or greater output low-ESR ceramic capacitor is required for stability..
13	FB2	Feedback Pin of LDO1. Receives the feedback voltage from a resistive divider connected across the output.
14	PGOOD2	Power Good Indicator of LDO1. Open-drain logic output that is opened when the output voltage exceeds 90% of the regulation point.
15	EN2	LDO1 Enable. A logical high level at this pin enables LDO1, while a logical low level causes LDO1 to shut down.
16	EN3	LDO2 Enable. A logic high level at this pin enables LDO2, while a logic low level causes LDO2 to shut down.
17	PGOOD3	Power Good Indicator of LDO2. Open-drain logic output that is opened when the output voltage exceed 90% of regulation point.
18	FB3	Feedback Pin of LDO2. Receives the feedback voltage from a resistive divider connected across the output.
19	AGND	Analog Grand. All small-signal of the IC should connect to this ground, which connects to PGND at one point for away exposed pad.
20	VOUT3	Output of LDO2. A 1uF or greater output low-ESR ceramic capacitor is required for stability.
21	VIN3	Power Input Supply of LDO2. Decouple this pin to GND with a 1uF or greater capacitor.
7, 10, 22	NC	No Internal Connection.
23	FB1	Feedback Pin of step-down converter. Receives the feedback voltage from a resistive divider connected across the output.
24	EN1	Step-down converter Enable. A logic high level at this pin enables step-down converter, while a logic low level causes step-down converter to shut down.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN1, VIN2 ---------- –0.3V to 6V
- Output Pin Voltage ---------- –0.3V to (V_{IN1} + 0.3V)
- PHASE Pin Voltage ---------- –0.3V to (V_{IN2} + 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  WQFN-24L 4x4, θ_{JA} ---------- 52°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, Converter ---------- 2.6V to 5.5V
- Supply Input Voltage, LDOs ---------- 2.4V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Step-down converter						
Input Voltage Range	V_{IN1}		2.6	--	5.5	V
Feedback Voltage	V_{FB1}		0.784	--	0.816	V
Under Voltage Lockout Threshold	V_{UVLO}	V_{DD1} Rising	2.24	2.36	2.48	V
		V_{DD1} Hysteresis	--	150	--	mV
DC Bias Current		Active, V_{FB} = 0.75V, Not Switching	--	300	--	μA
Shutdown Current	I_{SHDN}	EN2 = 0	--	--	2	μA
Switch On Resistance, High	R_{FET_H}	I_{PHASE} = 0.5A	--	150	270	mΩ
Switch On Resistance, Low	R_{FET_L}	I_{PHASE} = 0.5A	--	90	150	mΩ
Peak Current Limit	I_{LIM}		1.7	2.3	3.2	A
Switching Frequency			1	1.2	1.4	MHz
Output Voltage Line Regulation		V_{IN1} = 2.6V to 5.5V	--	0.01	1	%/V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Load Regulation		Measured by sever loop, EA output from 0.253V to 0.853V	--	0.01	1	%
FB Threshold for PGOOD Transition			0.68	0.72	0.76	V
PGOOD1 Pull-Down Resistance			--	--	100	Ω
EN1 Input High			1.4	--	--	V
EN1 Input Low			--	--	0.4	V
Thermal Shutdown Temperature	T_{SD}	(Note 5)	--	145	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	25	--	
LDO1 (V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1uF (Ceramic))						
Input Voltage Range	V_{IN2}		2.4	--	5.5	V
Feed Back Voltage	V_{FB2}		0.784	--	0.816	V
Output Noise Voltage	e_{NO}	V_{OUT2} = 1.5V, I_{OUT2} = 1mA	--	30	--	μV_{RMS}
Quiescent Current	I_Q	V_{EN2} = 5V, I_{OUT2} = 0mA	--	35	60	μA
Shutdown Current	I_{SHDN}	EN2 = 0	--	--	2	μA
EN2 Pin Current	I_{EN2}	Measured EN leakage current. EN2 = 5.5V	--	0.1	1	μA
Current Limit	I_{LIM}	R_{LOAD} = 0Ω	0.7	0.9	1.2	A
Dropout Voltage	V_{DROP}	I_{OUT2} = 500mA, V_{IN2} > 2.7V	--	250	400	mV
Load Regulation	ΔV_{LOAD}	1mA < I_{OUT2} < 500mA, V_{IN2} > 2.7V	--	1	--	%
Line Regulation	ΔV_{LINE}	V_{IN2} = (V_{OUT2} + 0.5) to 5.5V I_{OUT2} = 1mA	--	0.01	0.2	%/V
Power Supply Rejection Ratio, f = 100kHz	PSRR	I_{OUT2} = 300mA	--	40	--	dB
FB Threshold for PGOOD Transition			--	0.72	0.76	V
PGOOD2 Pull-Down Resistance			--	--	120	Ω
EN2 Input High			1.4	--	--	V
EN2 Input Low			--	--	0.4	V
LDO2 (V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1uF (Ceramic))						
Input Voltage Range	V_{IN3}		2.4	--	5.5	V
Feed Back Voltage	V_{FB3}		0.784	--	0.816	V
Output Noise Voltage	e_{NO}	V_{OUT3} = 1.5V, I_{OUT3} = 1mA	--	30	--	μV_{RMS}
Quiescent Current	I_Q	V_{EN3} = 5V, I_{OUT3} = 0mA	--	35	60	μA
Shutdown Current	I_{SHDN}	EN1 = 0	--	--	2	μA
EN3 Pin Current	I_{EN3}	Measured EN leakage current. EN3 = 5.5V	--	0.1	1	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	I_{LIM}	R_{LOAD} = 0Ω	0.35	0.48	0.6	A
Dropout Voltage	V_{DROP}	I_{OUT3} = 250mA, V_{IN3} > 2.7V	--	250	400	mV
Load Regulation	ΔV_{LOAD}	1mA < I_{OUT3} < 250mA, V_{IN3} > 2.7V	--	1	--	%
Line Regulation	ΔV_{LINE}	V_{IN3} = (V_{OUT3} + 0.5) to 5.5V I_{OUT3} = 1mA	--	0.01	0.2	%/V
EN3 Pin Current	I_{EN3}	Measured EN leakage current. EN3 = 5.5V	--	0.1	1	μA
Current Limit	I_{LIM}	R_{LOAD} = 0Ω	0.35	0.48	0.6	A
Dropout Voltage	V_{DROP}	I_{OUT3} = 250mA, V_{IN3} > 2.7V	--	250	400	mV
Load Regulation	ΔV_{LOAD}	1mA < I_{OUT3} < 250mA, V_{IN3} > 2.7V	--	1	--	%
Line Regulation	ΔV_{LINE}	V_{IN3} = (V_{OUT3} + 0.5) to 5.5V I_{OUT3} = 1mA	--	0.01	0.2	%/V
Power Supply Rejection Ratio, f = 100kHz	PSRR	I_{OUT3} = 150mA	--	40	--	dB
FB3 Threshold for PGOOD Transition			--	0.72	0.76	V
PGOOD3 Pull-Down Resistance			--	--	120	Ω
EN3 Input High			1.4	--	--	V
EN3 Input Low			--	--	0.4	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad of the package.

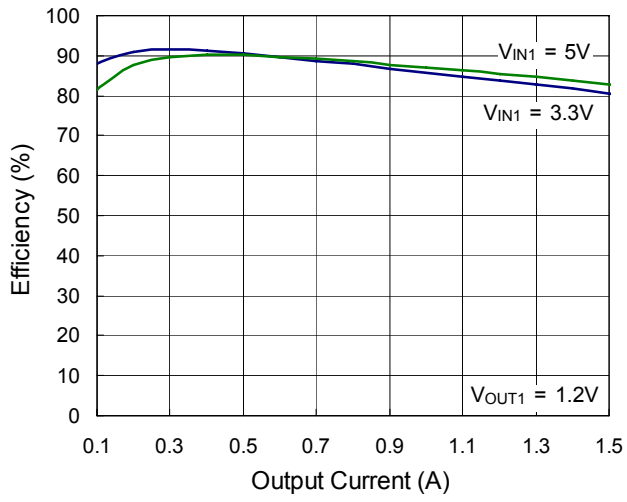
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

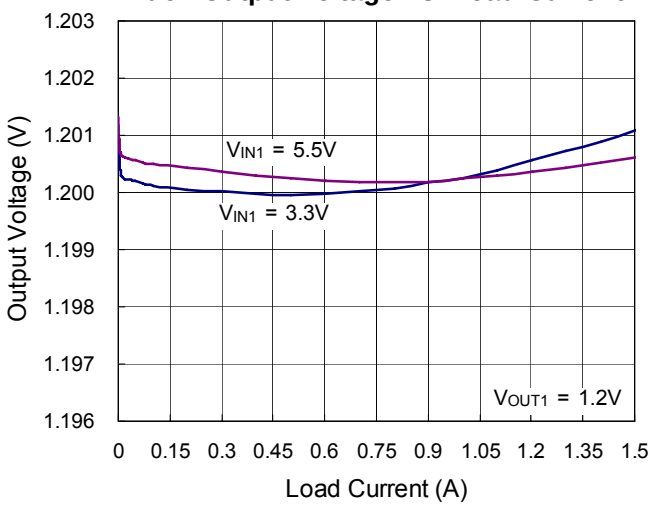
Note 5. The power source for thermal shutdown circuit must be provided by V_{IN1}. There must be a power input into LDO1 and then the LDO2 can provide the thermal shutdown function.

Typical Operating Characteristics

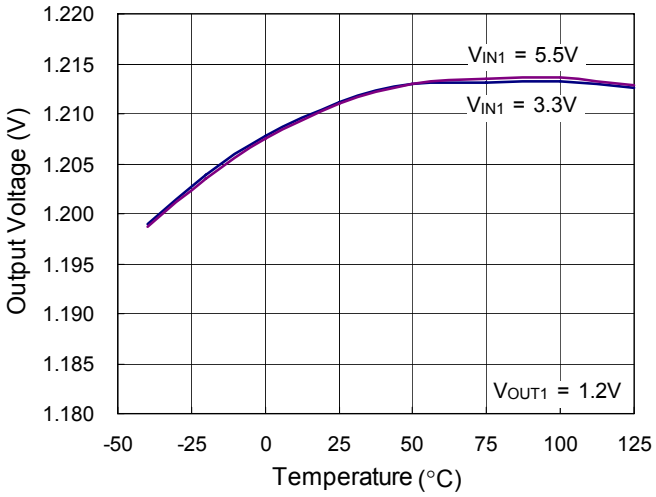
Buck Efficiency vs. Output Current



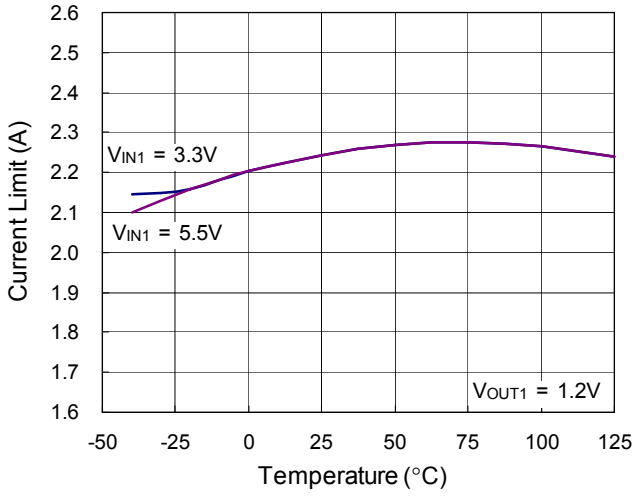
Buck Output Voltage vs. Load Current



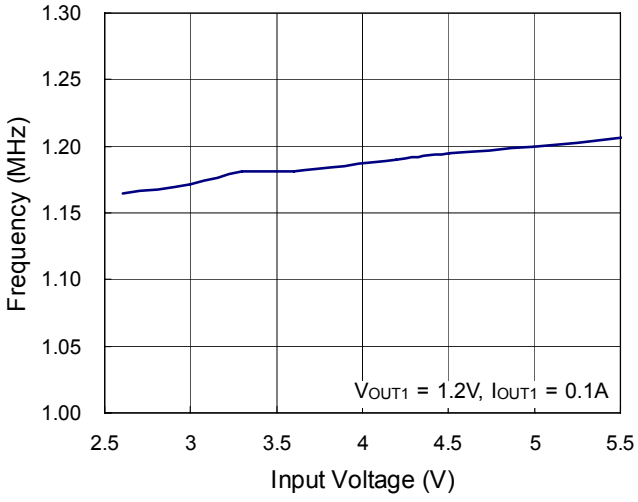
Buck Output Voltage vs. Temperature



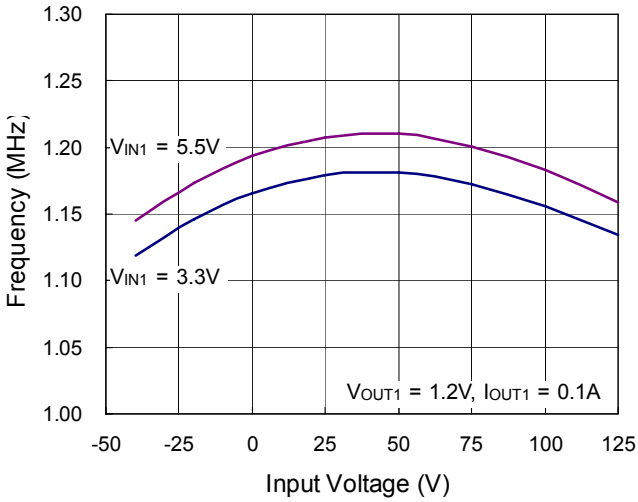
Buck Current Limit vs. Temperature



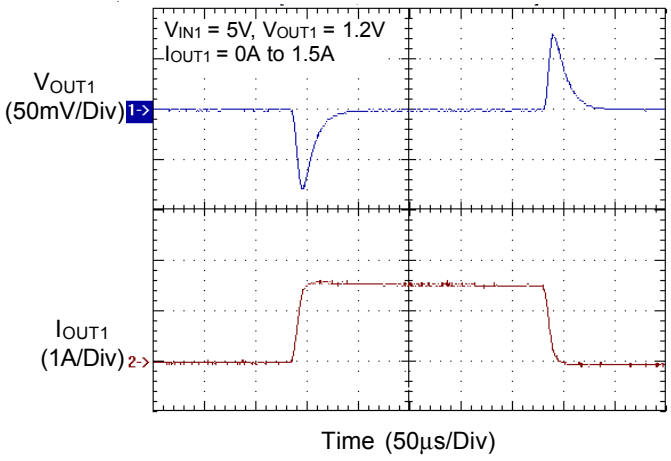
Buck Frequency vs. Input Voltage



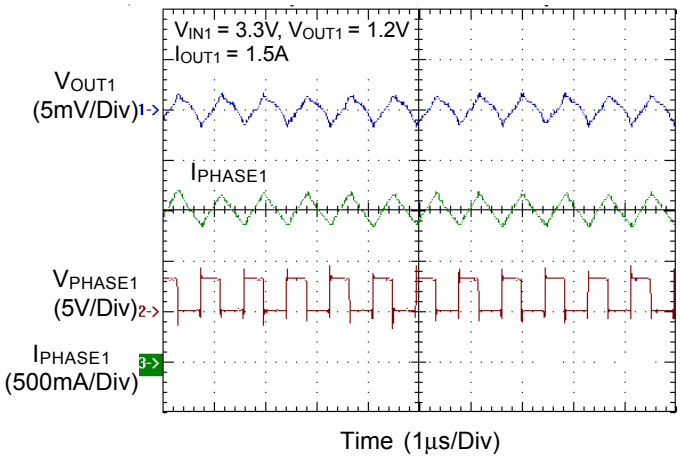
Buck Frequency vs. Input Voltage



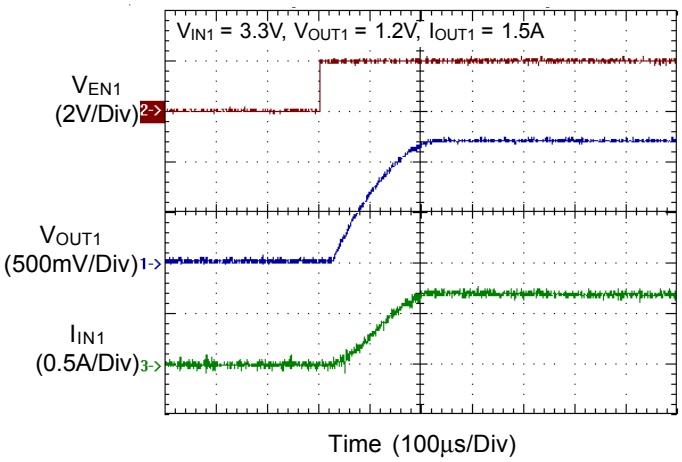
Buck Load Transient Response



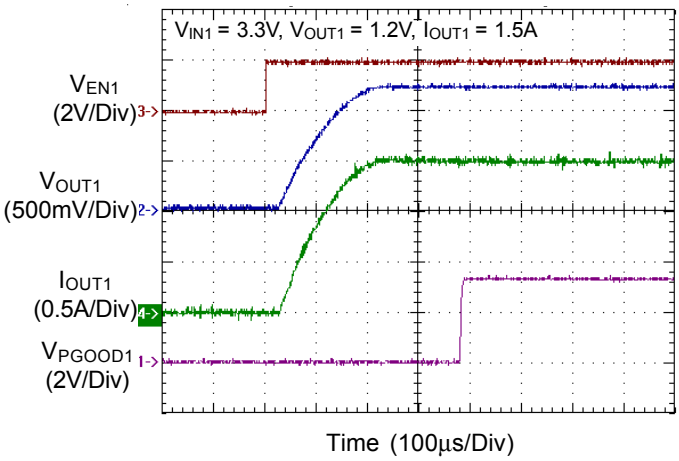
Buck Switching Waveforms



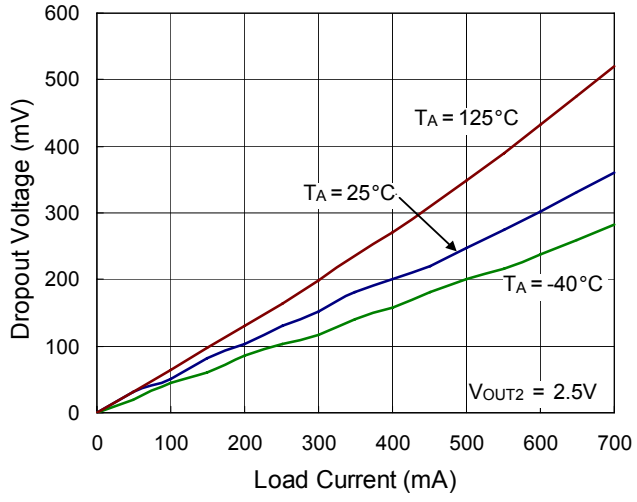
Buck Power On from EN



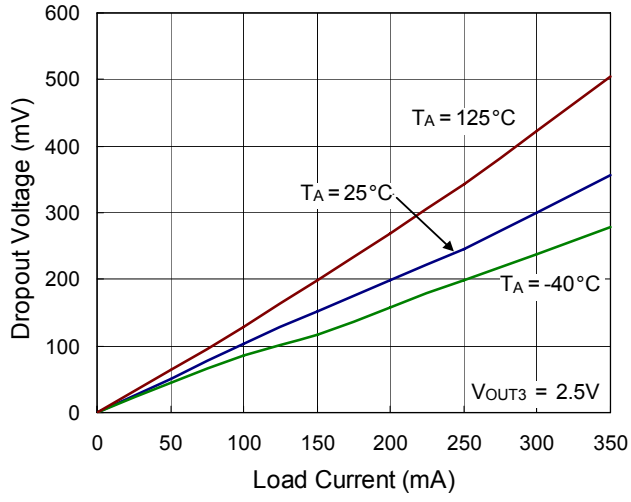
Buck PGOOD Response



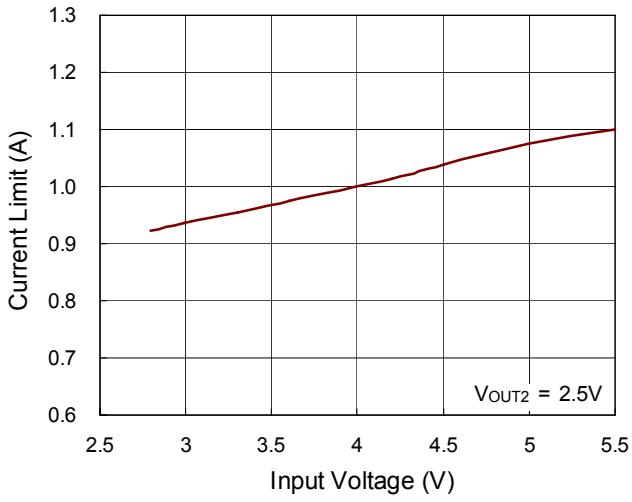
LDO1 Dropout Voltage vs. Load Current



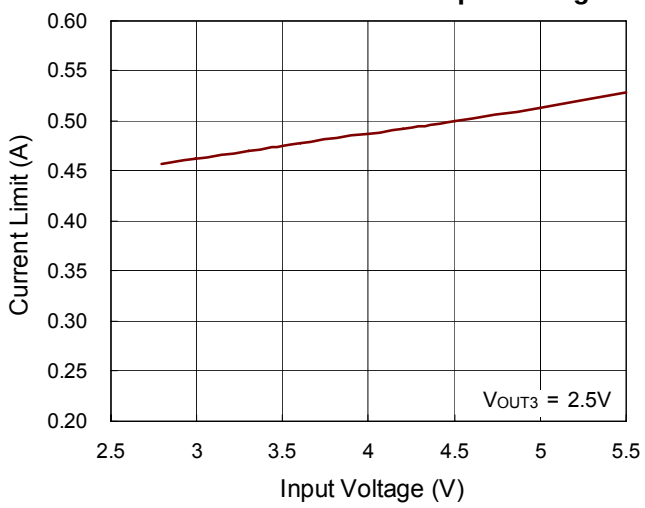
LDO2 Dropout Voltage vs. Load Current



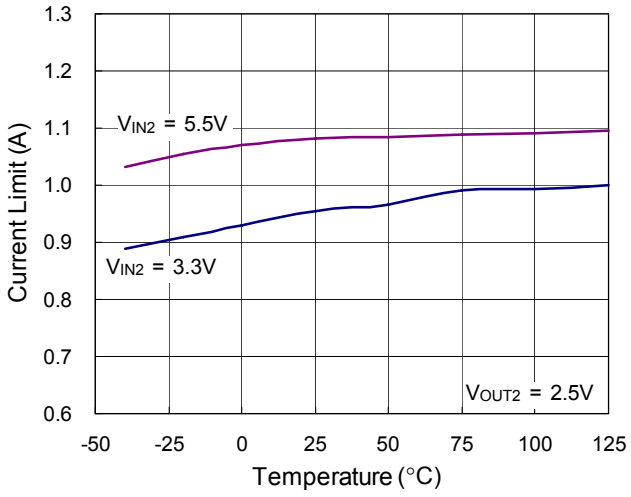
LDO1 Current Limit vs. Input Voltage



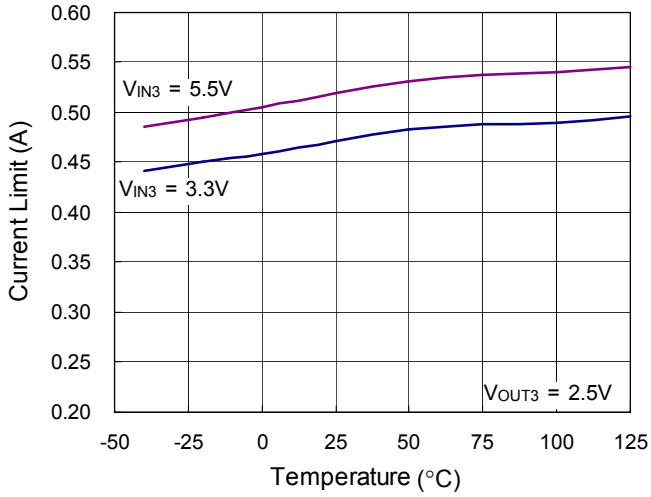
LDO2 Current Limit vs. Input Voltage



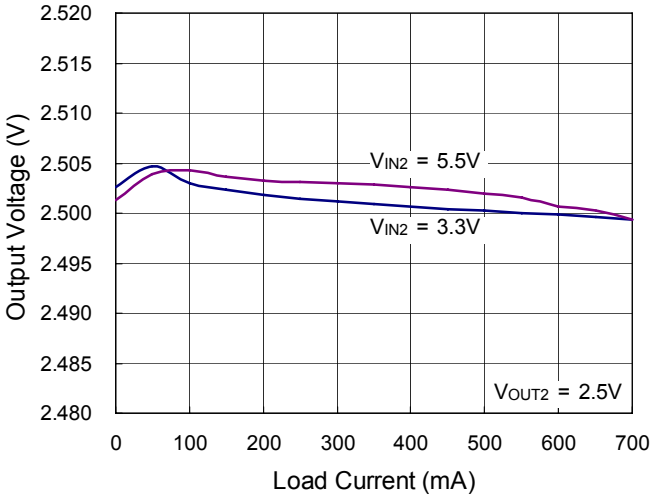
LDO1 Current Limit vs. Temperature



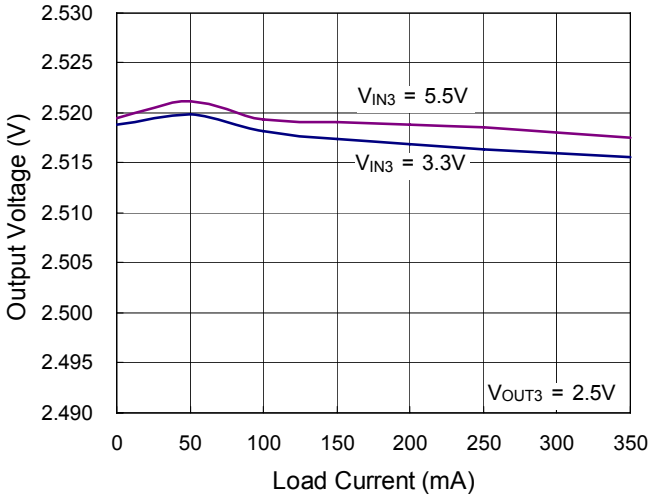
LDO2 Current Limit vs. Temperature



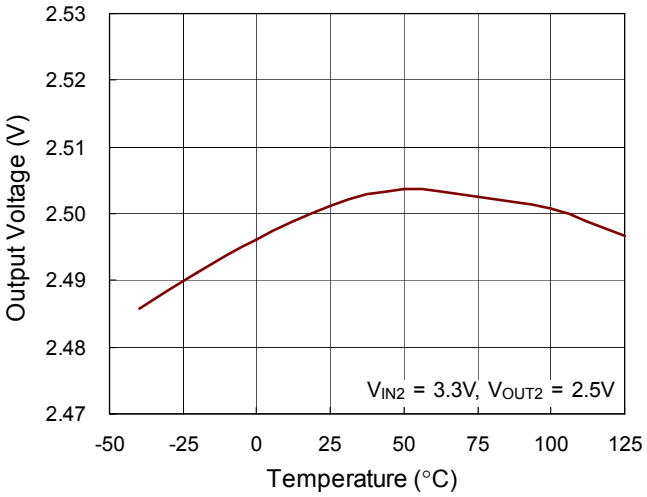
LDO1 Output Voltage vs. Load Current



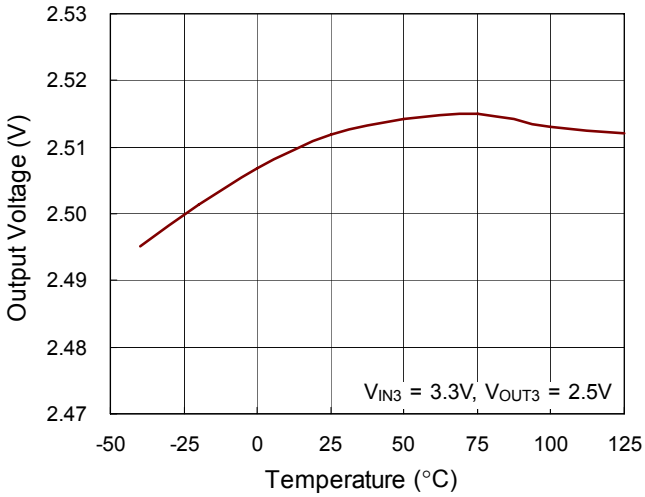
LDO2 Output Voltage vs. Load Current



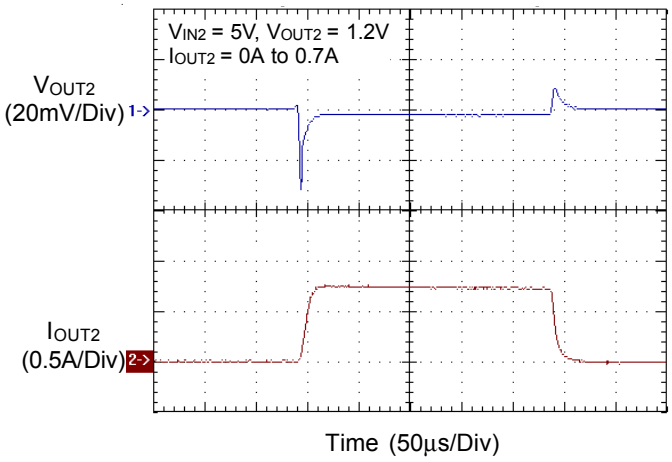
LDO1 Output Voltage vs. Temperature



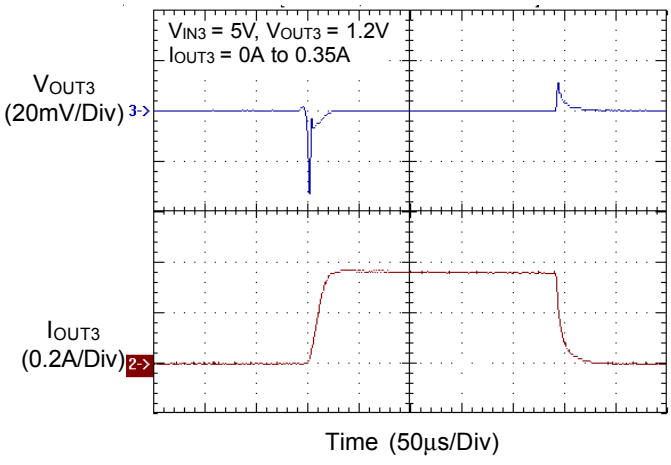
LDO2 Output Voltage vs. Temperature



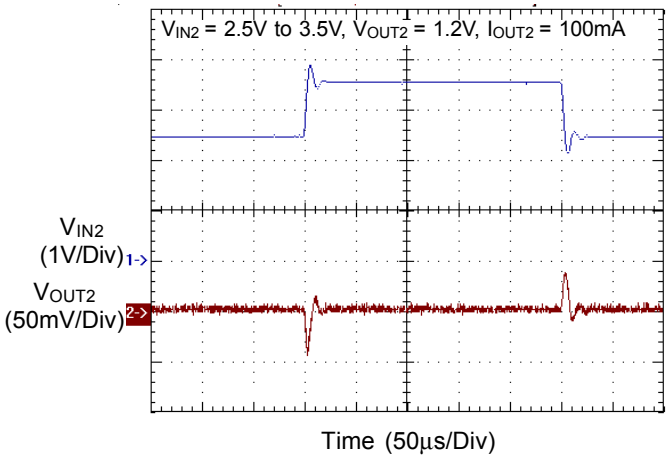
LDO1 Load Transient Response



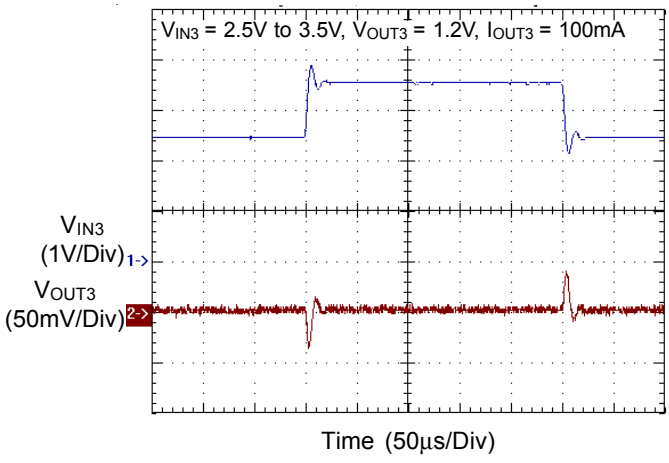
LDO2 Load Transient Response



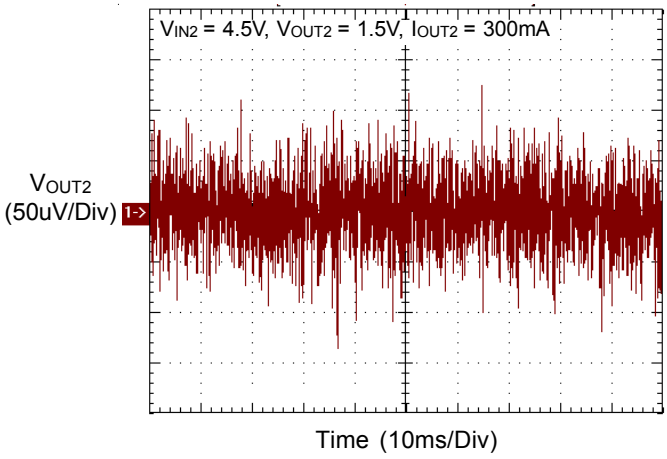
LDO1 Line Transient Response



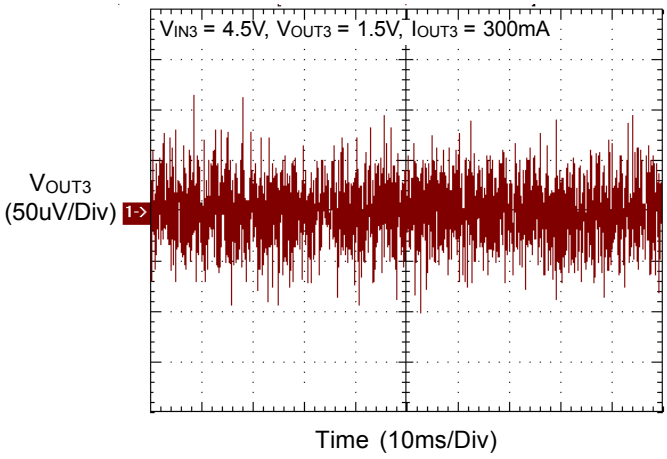
LDO2 Line Transient Response



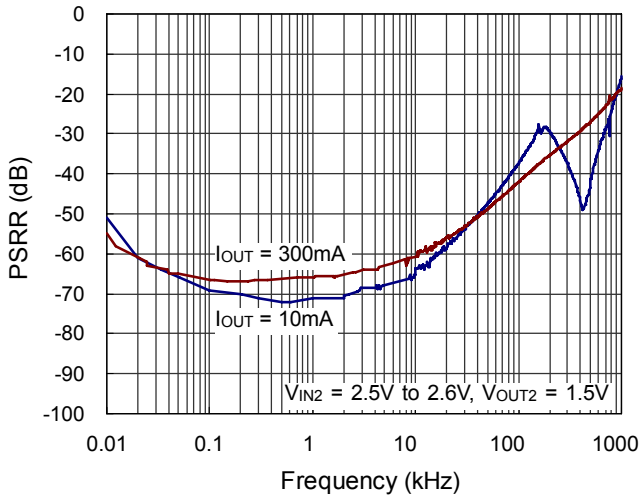
LDO1 Noise



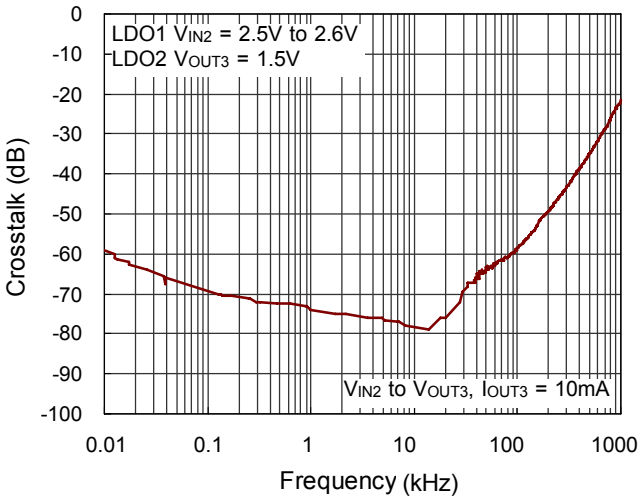
LDO2 Noise



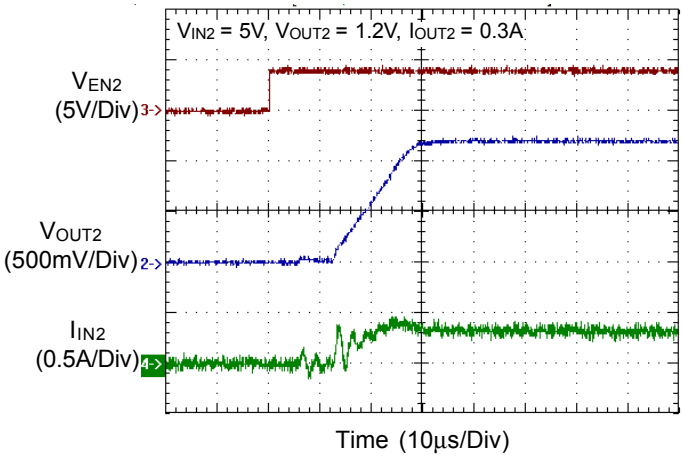
LDO1 PSRR



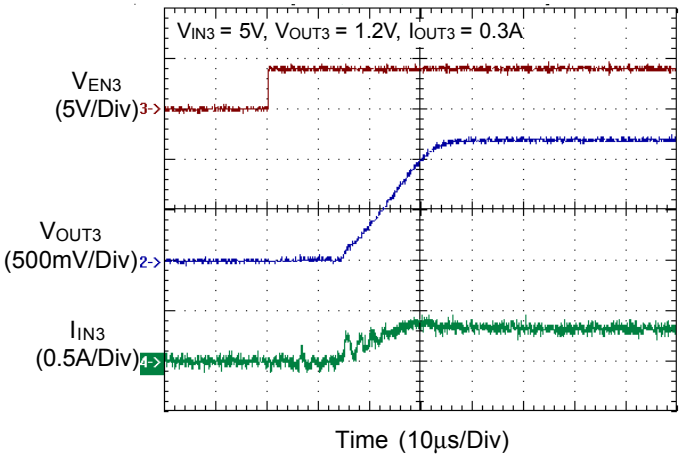
Crosstalk



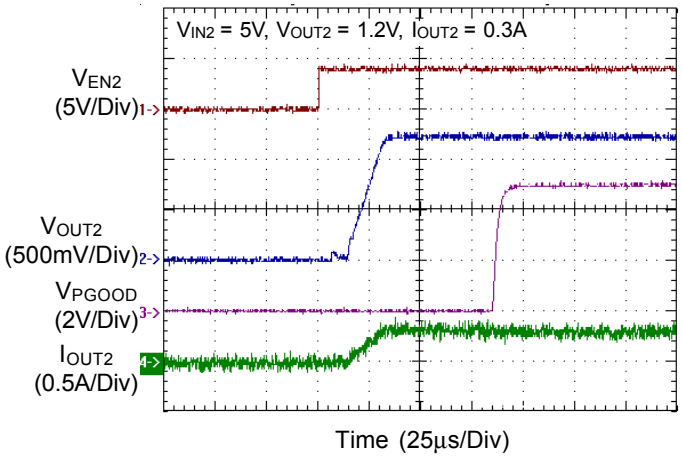
LDO1 Power On from EN2



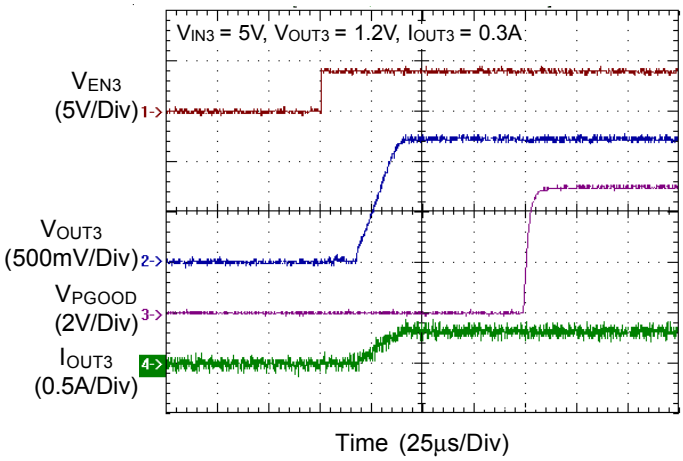
LDO2 Power On from EN3



LDO1 PGOOD Response



LDO2 PGOOD Response



Application Information

For Buck Converter Part

The Typical Application Circuit shows the basic RT8023 application circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

The inductor type must be selected once the value for L is known. Generally speaking, high efficiency converters can not afford the core loss found in low cost powdered iron cores. So, the more expensive ferrite or mollypermalloy cores will be a better choice. The selected inductance rather than the core size for a fixed inductor value is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increase of the inductance requires more turns of wire and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequency due to the characteristics of very low core losses. So, design goals can focus on the reduction of copper loss and the saturation prevention.

Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. The previous situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than the similar powdered iron inductors. The rule for inductor choice mainly depends on the price vs. size requirement and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the required effective series resistance (ESR) to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple will be highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure2.

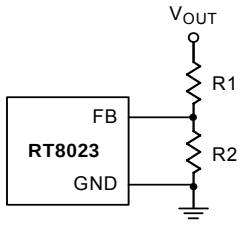


Figure 2. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the internal reference voltage (0.8V typ.).

Efficiency Consideration

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. The efficiency can be expressed as :

Efficiency = 100 – (L1 + L2 + L3 + …..)

Where L1, L2, etc., are the individual losses as a percentage of input power, although all dissipative elements in the circuit produce losses, V_{IN} quiescent current and I^2R losses are two main sources for most of the losses.

The V_{IN} quiescent current loss dominates the efficiency loss at a very low load current whereas the I^2R loss dominates the efficiency loss at medium to high load current. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current appears due to two factors including the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The value of $\Delta Q/\Delta t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG} = f(Q_T + Q_B)$

Where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and their effects will be more significant at higher supply voltages.

2. I^2R losses are calculated from the resistance of the internal switches R_{SW} and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFETs $R_{DS(ON)}$ and the duty cycle (DC) as follows :

$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristic curves. Thus, to obtain I^2R loss, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of total losses.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

For LDO Part

The external capacitors used with the RT8023 must be carefully selected for regulator stability and performance just like any low-dropout regulator.

Using a capacitor whose value is >1μF on the RT8023 input and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 1cm from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDO applications. The RT8023 is designed specifically to work with low ESR ceramic output capacitor for space-saving and performance consideration.

Enable

The RT8023 goes into sleep mode when the EN pin is in the logic low condition. The RT8023 has an EN pin to turn on or turn off the regulator during this condition. When the EN pin is in the logic high condition, the regulator will be turned on. The typical supply current for the EN pin is 0.1μA. The EN pin may be directly tied to V_{IN} to keep the part on. The enable input is CMOS logic and can not be left floating.

Current Limit

The RT8023 contains an independent current limiter to monitor and control the pass transistor's gate voltage. The part limits the two LDOs' current respectively as follows : LDO1 : 700mA and LDO2 : 350mA (min.). The output can be shorted to ground indefinitely without damaging the part.

PGOOD

The power good output is an open-drain output. It is designed essentially to work as a power-on reset generator once the regulated voltage was up or a fault condition occurs. The output of the power good drives to low when a fault condition occurs. The power good output will be driven back to up once the output reaches 90% of its nominal value. The output voltage level will be drooped at the fault condition including current limit, thermal shutdown or shutdown and triggers the PGOOD detector to alarm a fault condition.

Due to the shutdown mode condition, a fault condition occurs by pulling up the PGOOD output low. And it will sink a current from the open drain and the external power.

It is recommended to select a suitable pulling resistance to achieve the goal of ideal power dissipation control.

PSRR

The power supply rejection ratio (PSRR) is defined as the ability of a regulator to maintain its output voltage as its power supply voltage is varied. The PSRR is found to be:

$PSRR = 20 \times \log[\Delta V_{OUT}/\Delta V_{IN}]$

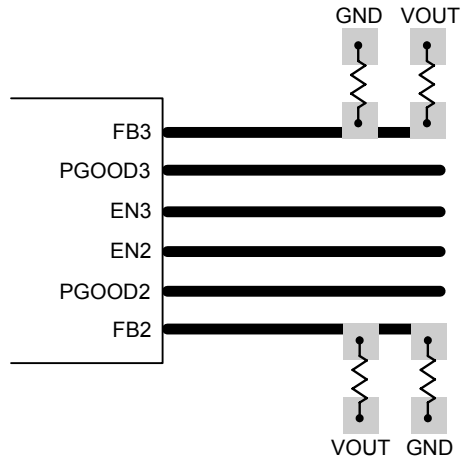


Figure 3

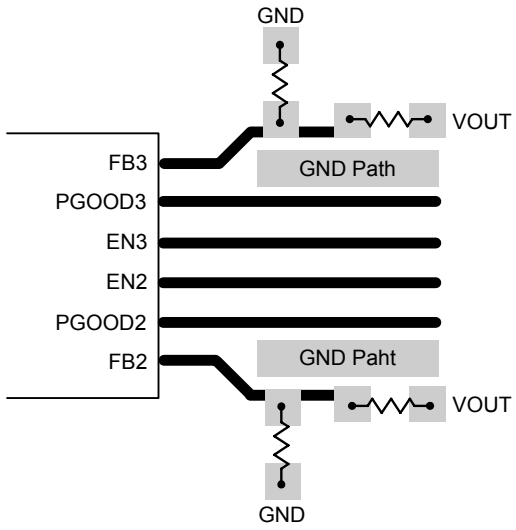


Figure 4

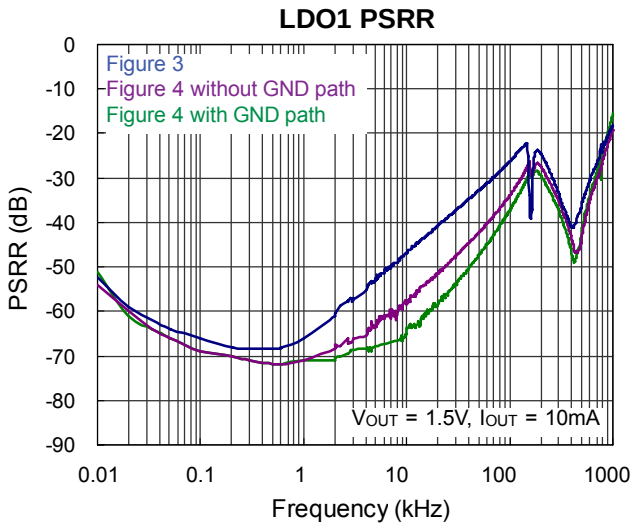


Figure 5. The PSRR for the RT8023

Note : The temperature effect must be taken into consideration for heavy load PSRR measuring.

How a PCB layout will affect the PSRR is shown as Figure 3. If the FB is placed in parallel with the PGOOD and EN, the output voltage will be interfered to result in a bad PSRR performance that is shown as Figure 5.

For the layout as shown in Figure 4, the FB is separated from the PGOOD and the EN. In this condition, there will be less interference for the output voltage and it will lead to a better PSRR performance.

As shown in Figure 5, if the FB is separated from the PGOOD and EN and a GND path is added, then it will lead to a better PSRR performance especially for high frequency applications.

Thermal Consideration

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operating junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8023, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance

θ_{JA} is layout dependent. For WQFN-24L 4x4 packages, the thermal resistance θ_{JA} is 52°C/W on the standard JEDC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 52°C/W = 1.923 for WQFN-24L 4x4 packages.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} For RT8023 packages, the Figure 6 of derating curves allows the designer to see the effect of rising ambient temperature of maximum power allowed.

Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT 8023

- Please refer to the PSRR section for layout improvement.
- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8023. For the LDO layout part, put the output capacitor as close as possible to the device pins. (VIN and GND).
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

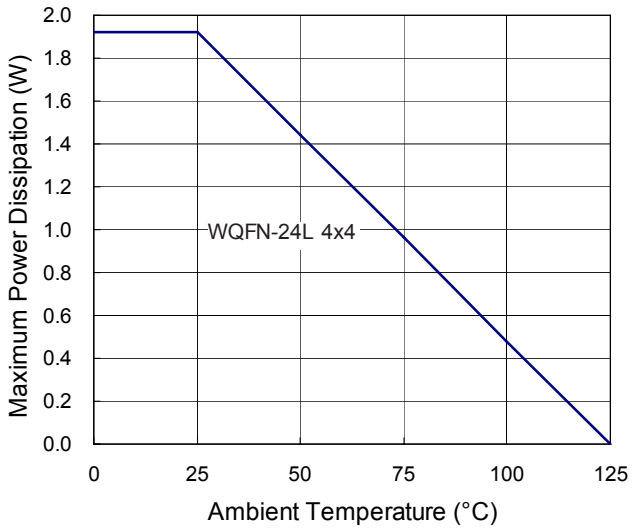


Figure 6. Derating Curves for RT8023 Packages

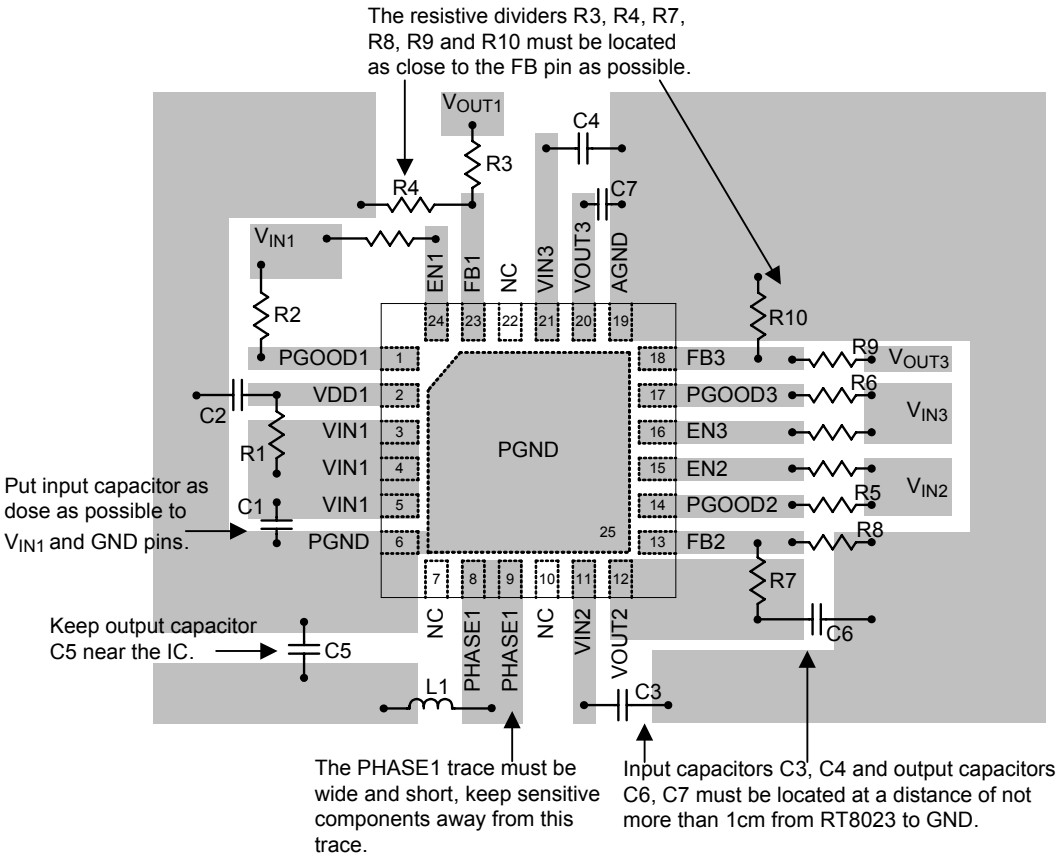
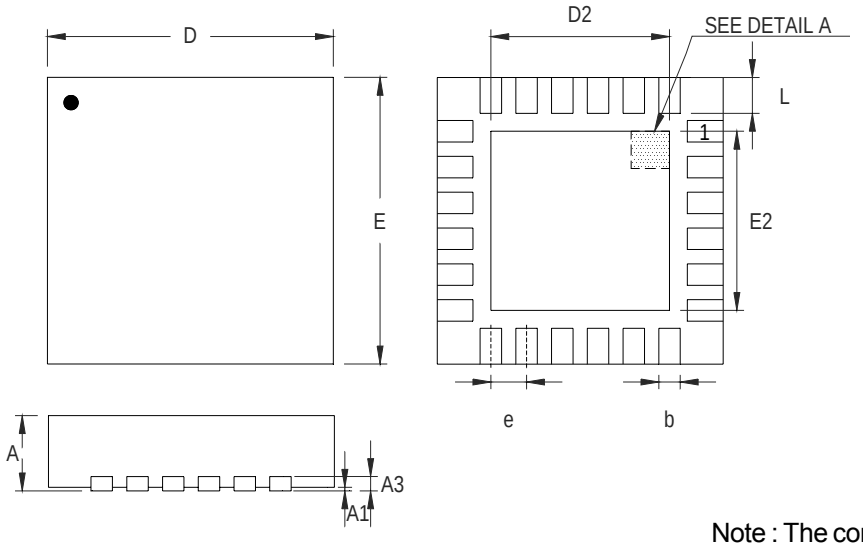
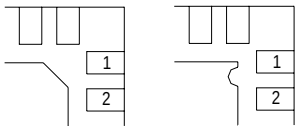


Figure 7

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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